Response To Office Action Mailed July 5, 2005

A. Pending Claims

Claims 1-6 are pending. Claim 1 has been amended.

A. Drawings

In the Office Action, it was indicated that the drawings were filed on March 22, 2004, however, it was not indicated whether the drawings were accepted or objected to by the Examiner. Applicant respectfully requests the Examiner to indicate whether the drawings are acceptable or not acceptable in their current form.

C. The Claims Are Not Obvious Over EP 1187308 In View of Yu Pursuant to 35 U.S.C. § 103(a)

Claims 1-6 were rejected under 35 U.S.C. § 102(e) as being obvious over EP 1187308 to Jacques Majos ("EP 1187308") in view of U.S. Patent No. 5,793,096 to Yu et al. ("Yu"). Applicant submits that the claims are patentable over the cited art.

The Office Action states:

> The EP1187308 reference shows in Figure 2 the substantially the same figure as in Figure 1 of this application and shows every structure limitation in the claims. However, the reference does not disclose the physical structure arrangement of the inductor as recited, "therein the inductors of the oscillating circuits are produced in MOS technology and are superimposed one on top of the other". Yu et al. discloses a spiral inductor in which MOS transistors are internally installed using multi-layer metallization technology and teaches that this technology provides reduction of the chip area. In order to further reduce the chip area, it would have been obvious to one of ordinary skill in the art to recognized that two inductors be superposed one on top of the other because such a modification would have provided the benefit of further reducing the chip area. (Office Action, page 2)

Claim 1 includes a combination of features including, but not limited to, the features of:

> comprising an oscillating stage with two coupled CMOS inverters forming a quadrupole with two inputs and with two outputs; and
>
> the quadrupole being configured such that the outputs of the quadrupole are in phase, wherein the inductors of the oscillating circuits are produced in MOS technology and are superposed one on top of the other thereby allowing the inductor chip area to be reduced as a function of the mutual inductance coefficient of the stacked inductors.

Applicant's Specification states:

> It should be noted that the mutual inductance between the two inductors allows the properties of the oscillator to be modified. This is because, in a configuration with stacked inductors, if each inductor has an inductance value L, because of the coupling between these two inductors, each inductance value L' then becomes:
>
> $$L' = L(1+k)$$
>
> where k denotes the coefficient of mutual inductance of the two inductors.
>
> It will be consequently understood that, using such a structure of stacked inductors for the implantation of the inductors L1 and L2, if the coefficient k of mutual inductance is close to 1, the inductance value of each inductor is doubled, thereby making it possible to half the diameter of each inductor. (Applicant's Specification, page 8, lines 1-14)

In the Office Action, the Examiner agrees that EP 1187308 does not appear to teach or suggest "inductors of the oscillating circuits are produced in MOS technology and are superimposed one on top of the other." Applicant submits that Yu also does not appear to teach or suggest at least the quoted feature of the claim. Yu states:

> in the present invention, the MOS transistors having a channel width of 4xW μm are disposed under the inductor, and therefore, there is not needed a separate area for the MOS transistors, with the result that the chip area is greatly reduced." (Yu, col. 3, lines 32-35)

Yu does not appear to teach or suggest superimposing inductors one on top of the other. Yu appears to teach superposing an inductor onto transistors, which reduces the chip area since a separate area for the MOS transistors is no longer necessary. Consequently, Yu does not appear

to teach or suggest saving more area than either the inductor area or the transistors area. Yu does not appear to teach or suggest superimposing inductors one on top of the other that allows the inductor chip area to be reduced as a function of the mutual inductance coefficient of the stacked inductors.

Applicant submits that EP 1187308 and Yu do not appear to teach or suggest at least the quoted features of claim 1. Applicant respectfully requests removal of the rejection to claim 1 and the claims dependent thereon.

Furthermore, Applicant respectfully disagrees that Figure 2 of EP 1187308 is substantially similar to Figure 1 of Applicant's Specification. Figure 2 of EP 1187308 appears to show that the inductors L1, L2 of the oscillator are physically separated by the quadripole 110 and transistors M1 to M4. The inductors of EP 1187308 do not appear to be mutually coupled. Applicant submits that Figure 1 of the Applicant's Specification does not appear to be substantially similar to Figure 2 of EP 1187308.

The Office Action included a rejection of claim 2 in view of the cited art. Claim 2 includes the feature of "wherein the inductors of the oscillating circuits are produced in the form of spirals implanted in respective metallization levels of an integrated circuit" in combination with the features of claim 1. Applicant respectfully submits that the cited art does not teach or suggest the features in claim 2 in combination with the features of claim 1.

The Office Action stated "[r]egarding claim 3, as an obvious consequence of two spiral inductors being superposed one on top of the other using an insulator such as thin oxide film in between two inductors, spiraled capacitors are formed." (Office Action, page 3) Claim 3 includes the feature of "wherein the inductors are in the form of spiraled capacitors formed respectively by metal implantation in the metallization levels that are isolated by a thin oxide film" in combination with the features of claim 1. Applicant submits that the cited art does not appear to teach or suggest inductors superposed one on top of the other where the inductors are in

the form of spiraled capacitors formed by metal implantation in the metallization levels that are isolated by a thin oxide film.

The Office Action included a rejection of claim 4 in view of the cited art. Claim 4 includes the feature of "wherein each inverter comprises two oppositely biased MOS transistors placed in line, the input of the inverters being located on the gate of one of the transistors having a first bias and the output at the mid-point of the two transistors" in combination with the features of claim 1. Applicant respectfully submits that the cited art does not teach or suggest the features in claim 4 in combination with the features of claim 1.

The Office Action included a rejection of claim 5 in view of the cited art. Claim 5 includes the feature of "wherein the input of each inverter is coupled to the gate of a transistor with a second bias of the other inverter, the said second bias being opposite that of the said first bias" in combination with the features of claim 1. Applicant respectfully submits that the cited art does not teach or suggest the features in claim 5 in combination with the features of claim 1.

The Office Action included a rejection of claim 6 in view of the cited art. Claim 6 includes the feature of "an amplification stage comprising two oppositely biased MOS transistors placed in series, the gate of each MOS transistor being coupled to one of the outputs of the oscillating stage" in combination with the features of claim 1. Applicant respectfully submits that the cited art does not teach or suggest the features in claim 6 in combination with the features of claim 1.

J. Additional Comments

Applicant submits that all claims are in condition for allowance. Favorable reconsideration is respectfully requested.

If any extension of time is required, Applicant hereby requests the appropriate extension of time. If any fees are required or if any fees have been overpaid, please appropriately charge or credit those fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5972-00400/EBM.

Respectfully submitted,

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